Processor Architecture: From Dataflow to Superscalar and Beyond

Von Jurij Silc, Borut Robic, Theo Ungerer
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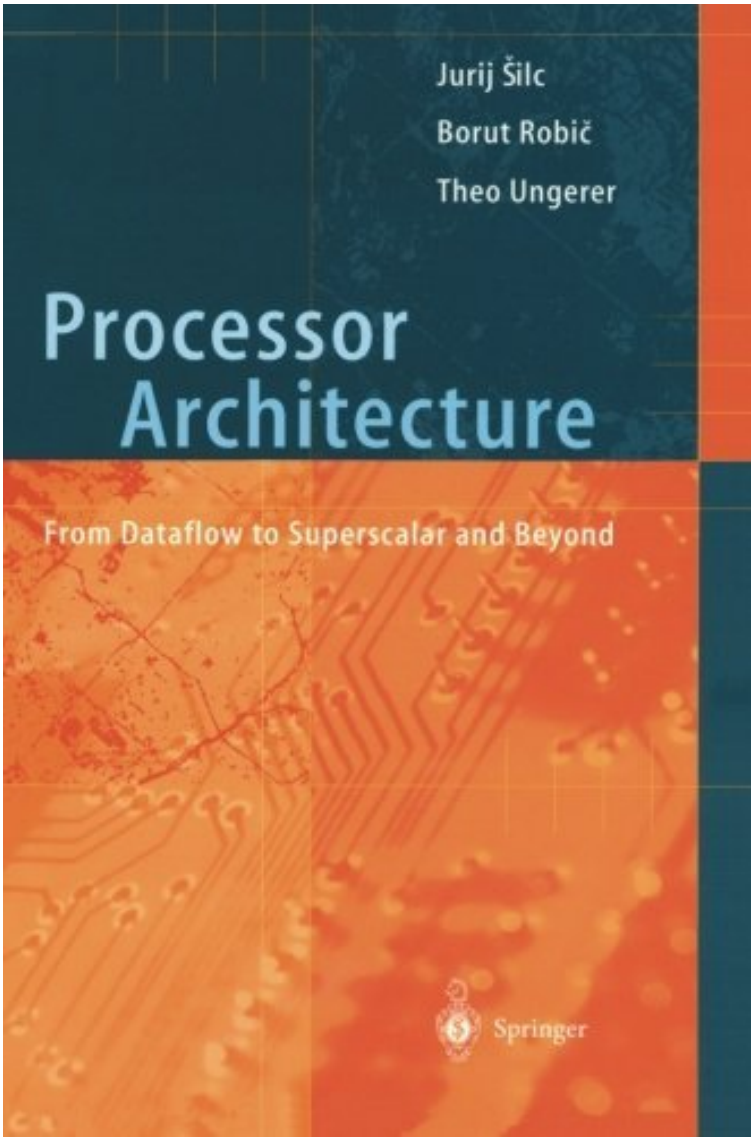

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Von Jurij Silc, Borut Robic, Theo Ungerer : Processor Architecture: From Dataflow to Superscalar and Beyond before purchasing it in order to gage whether or not it would be worth my time, and all praised Processor Architecture: From Dataflow to Superscalar and Beyond:

KundenrezensionenHilfreichste Kundenrezensionen3 von 3 Kunden fanden die folgende Rezension hilfreich. Ein zu diesem Thema sehr zufrieden stellendes BuchVon Ein KundeEin gutes Nachschlagewerk wenn man sich nher mit der Thematik der Prozessorarchitektur beschftigt. Es werden alle klassischen Architekturen wie CISC, VLIW und RISC

grundlegend bespochen und vertieft. Selbst Datenfluss Architekturen kommen hier, was eher selten ist, zu Ehren. Anschlieend wird die Funktionsweise superskalarer Architekturen ausfhrlich besprochen. Letzendlich wird auf zukunftstrchtige Ideen in der Prozesorarchitektur, wie reconfigurable computing und asynchrone Prozessoren eingegangen. Die Zielgruppe des Buches sind Forscher, interessierte Studenten der technischen Informatik und Ingenieure der Elektrotechnik/Technischen Informatik.

KurzbeschreibungA survey of architectural mechanisms and implementation techniques for exploiting fine- and coarse-grained parallelism within microprocessors. Beginning with a review of past techniques, the monograph provides a comprehensive account of state-of-the-art techniques used in microprocessors, covering both the concepts involved and implementations in sample processors. The whole is rounded off with a thorough review of the research techniques that will lead to future microprocessors. XXXXXXX Neuer Text This monograph surveys architectural mechanisms and implementation techniques for exploiting fine-grained and coarse-grained parallelism within microprocessors. It presents a comprehensive account of state-of-the-art techniques used in microprocessors that covers both the concepts involved and possible implementations. The authors also provide application-oriented methods and a thorough review of the research techniques that will lead to the development of future processors.KurzbeschreibungA survey of architectural mechanisms and implementation techniques for exploiting fine- and coarse-grained parallelism within microprocessors. Beginning with a review of past techniques, the monograph provides a comprehensive account of state-of-the-art techniques used in microprocessors, covering both the concepts involved and implementations in sample processors. The whole is rounded off with a thorough review of the research techniques that will lead to future microprocessors. XXXXXXX Neuer Text This monograph surveys architectural mechanisms and implementation techniques for exploiting fine-grained and coarse-grained parallelism within microprocessors. It presents a comprehensive account of state-of-the-art techniques used in microprocessors that covers both the concepts involved and possible implementations. The authors also provide application-oriented methods and a thorough review of the research techniques that will lead to the development of future processors.Synopsis This monograph surveys architectural mechanisms and implementation techniques for exploiting fine-grained and coarse-grained parallelism within microprocessors. It starts with a review of past techniques, continues with a comprehensive account of state-of-the-art techniques used in microprocessors that covers both the concepts involved and implementations in sample processors, and ends with a thorough review of the research techniques that will lead to future microprocessors.